



**SITAM**

**Satya Institute of Technology And Management**

NAAC ACCREDITED

Approved by AICTE,  
New Delhi and Govt. of A.P. Affiliated to JNTU  
K, KAKINADA

Gajularega, Kondakarakam (P.O), Vizianagaram –  
535003 Contact: 9676788811/9885758562, 08922-234775/9

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JNTUK Code: B6

EAMCET Code: SGVP

**Qualitative Metrics**

**Criterion VI - Governance, Leadership, and Management**

**6.5.2 The institution reviews its teaching-learning process, structures & methodologies of operations and learning outcomes at periodic intervals through IQAC set up as per norms and recorded the incremental improvement in various activities.**

SITAM-IQAC periodically reviews the teaching-learning process, structures & methodologies of operations, and learning outcomes: The standard methods of teaching, learning, and evaluation which are proven over the years are being followed:

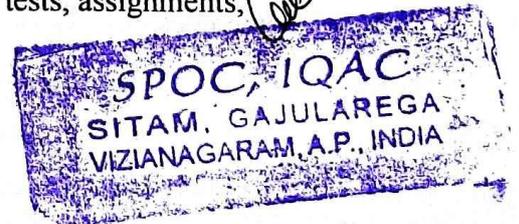
**Preparation of lesson plan for each Semester:** The lesson plan is prepared by the faculty members for all the subjects they teach in that particular semester. Enriching the curriculum with guest lectures, industrial visits, and Internships is also planned at this stage.

**Daily lecture Record:** Everyday faculty prepares and submit details of the lecture along with the topic covered on an online portal as well as Course Track Register (CTR).

**Evaluation of teachers by students:** The institution has a feedback system to check the quality of teaching. The regular evaluation of the teachers by the students, feedback on teaching methodologies, course delivery, attitude, strengths and weaknesses, difficulties faced in the subject give a clear idea about the problems faced by the students. Director and management also monitor the feedback system and takes appropriate corrective actions.

**Student learning outcomes:** The institute monitors the performance of the students regularly. It has specified procedure to collect and analyze data on student learning outcomes; the following points are adopted by the institute in this context:

- Midterm and continuous evaluation comprising of internal tests, assignments, group discussions, and seminar presentations.
- Regular class tests and interactions
- Semester system of examination for all courses.
- Providing Lecture notes through an online portal
- Timely Redressal of student's grievances.
- Extra classes for challenged students to address their concerns.



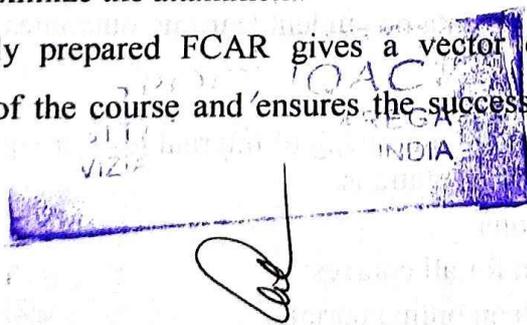
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**Effective internal examination and evaluation systems:** Institute maintains an effective internal examination and evaluation system.

**Faculty Course Assessment Report (FCAR):** SITAM, under the aegis of affiliating university, JNTUK, follows Outcome Based Education (OBE) to meet the standards of NAAC. As a part of the OBE:

- ✓ Well laid Course Outcomes (CO) and Program Outcomes (PO) along with a careful mapping process completely define the capabilities that a student graduating out of the program must possess. These are carefully reviewed by the Board of Studies (BoS) at the university level and are provided by JNTUK to SITAM.
- ✓ SITAM, based on the requirements stipulated in the OBE framework provided by the JNTUK, prepares its lesson plans along with requisite interventions needed to meet all the specifications of the OBE precepts.
- ✓ Once these are prepared, the teachers prepare their lecture notes and any other tools needed for imparting the capability specified in the CO-PO framework. Formative Examinations (FE) and Summative Examinations (SE) carefully evaluate the depth of understanding and capability of students.
- ✓ The results of these FE and SE give a wealth of results for the overall measure of the Course Outcome Attainment (COA). The COA calculations are mandatorily performed by the teachers of SITAM and are presented in the form of FCAR. In essence, FCAR lists:
  - The COs and the POs to which the COs map.
  - List of questions/components in the examination/tool of assessment and the CO-PO underlying the questions.
  - Scores of all the students
  - Calculation of the CO and the PO giving the attainment values computed using standard procedures.
  - An analysis of the attainment values and indication of the future directions which maximize the attainment.
- ✓ A carefully prepared FCAR gives a vector direction for the improvement in future instances of the course and ensures the success of the students in attaining the specified outcomes.



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**Students' result analysis:** Institute has the provision of analysis of students' performance after the announcement of their semester results. If the result of the students, in a subject, is not found up to the mark, necessary steps are taken to find out the reasons and the concerned faculty members are counselled and motivated to work towards improvement.

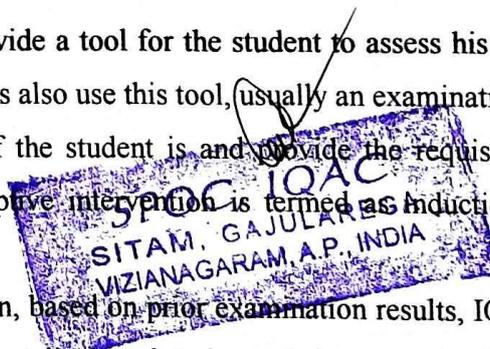
**Parent's Meet:** Regular parent-teacher meeting is conducted once in a semester to enable discussion, obtaining parent feedback and taking improvement measures.

**Mentoring System:** One of the first steps IQAC took up was to institute a mentoring system into place. Each teacher is assigned about 15 students as a mentees. The idea was that the teacher acts as friend, philosopher, brother/sister, guide, helper, mentor, and as an inside-person to provide assistance to the mentees in his group to the best possible extent. Thus, the mentor provides both academic and moral support to the student to ensure all round growth of the student. Each mentor:

- Keeps complete record of academic and other related history of the student in a Mentor's Diary.
- Meets and encourages students on a periodic basis to ensure correct trajectory for all round growth of the student.
- Maintains contact with the parents and gains their confidence to ensure proper ambience and support from family.
- Provides counseling where it is needed by the student in difficult times.
- Attempts to coordinate with training placement officer to ensure fullest support for his mentee.

**Remedial Classes:** Another important initiative of IQAC is to practice the concept of remediation in all aspects. Owing to the background and innate inclination, some students may falter a little bit in one or more area. It is the duty of the institute to provide help to such students and ensure their success. IQAC initiated this activity by planning and preemptive approaches. In specific, IQAC set the following plan in motion:

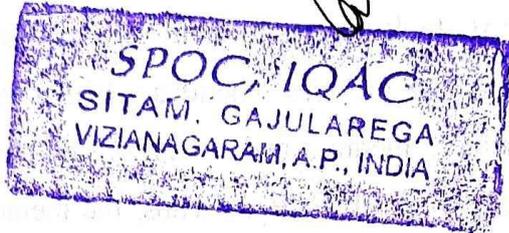
- At the time of admission, provide a tool for the student to assess his strengths and seek appropriate help. Teachers also use this tool, (usually an examination of sorts, to see what the specific need of the student is and provide the requisite input. The whole process of this preemptive intervention is termed as induction training in higher education parlance.
- During the examination season, based on prior examination results, IQAC institutes personalized assistance to hostellers and today scholars as per their need and convenience. This may be termed as help for summative assessment.
- After the examinations, if a student finds it difficult to clear the examination remedial classes are arranged so that student can surmount the difficulty with expert help from the teacher. This teacher may be the mentor of the student or another teacher whose help is requested by the mentor.



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**Teacher Peer Learning:** SITAM follows a unique concept of Teacher Peer Learning where in keen parameters of teacher feedback like Teachers Preparation for class, voice ,handwriting on black board, punctuality to the class , etc. are collected from students as well as colleagues necessary measures are taken as per the feedback for improvement.



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A Sample Lesson Plan is attached below,



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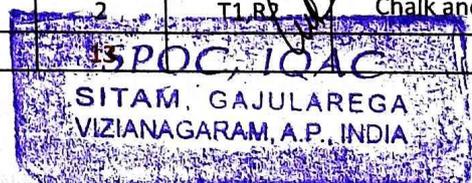
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<b>Program</b>	: U.G	<b>Branch</b>	: EEE		
<b>Course</b>	: B.TECH	<b>Subject</b>	: Digital Electronics		
<b>Academic Year</b>	: 2021-22 (II Year II Semester)	<b>Faculty Name</b>	: Mrs.V.N.Sireesha		
<b>LESSON PLAN</b>					
<b>Course Objectives:</b> To solve a typical number base conversion and analyze new error coding techniques, Theorems and functions of Boolean algebra and behaviour of logic gates, To optimize logic gates for digital circuits using various techniques, To understand concepts of combinational circuits, To develop advanced sequential circuits.					
S.No	Proposed Date	Unit No. & Topics to be covered	Required No. of Periods	Reference Text Books	Nature of Teaching
<b>UNIT – I Review of Number Systems &amp; Codes</b>					
1	07/03/22	Representation of numbers of different radix, conversion from one radix to another radix	3	T1,R1	Chalk and Talk
2	12/03/22	r-1's compliments and r's compliments of signed numbers	3	T1,R1	Chalk and Talk
3	16/03/22	Gray codes, 4 bit codes, BCD, Excess-3, 2421, 8421,	2	T1,R1	Chalk and Talk
4	19/03/22	Error detection & correction codes: parity checking, even parity, odd parity, Hamming code.	2	T1,R1	Chalk and Talk
5	21/03/22	Boolean theorems, principle of complementation & duality, De-Morgan theorems.	2	T1,R1	Chalk and Talk
6	23/03/22	Logic operations; Basic logic operations -NOT, OR, AND, Universal Logic operations, EX-OR, EX-NOR operations.	1	T1,R1	Chalk and Talk
7	26/03/22	Standard SOP and POS Forms	2	T1,R1	Chalk and Talk
8	28/03/22	NAND-NAND and NOR-NOR realizations.	2	T1,R1	Chalk and Talk
<b>Total Number of Classes for Unit-1</b>			<b>17</b>		
<b>Unit 2: Minimization Techniques</b>					
13	30/03/22	Minimization and realization of switching functions using Boolean theorems, K-Map (up to 6 variables)	4	T1,R2	Chalk and Talk
14	04/04/22	Tabular Method.	2	T1,R2	Chalk and Talk
15	06/04/22	Design of Half adder, full adder	1	T1,R2	Chalk and Talk
16	09/04/22	Half subtractor, full subtractor	1	T1,R2	Chalk and Talk
17	11/04/22	4- bit adder-subtractor circuit,	1	T1,R2	Chalk and Talk
18	12/04/22	BCD adder circuit,	1	T1,R2	Chalk and Talk
19	13/04/22	Excess 3 adder circuit	1	T1,R2	Chalk and Talk
20	16/04/22	Carry look-a-head adder circuit	2	T1,R2	Chalk and Talk
<b>Total Number of Classes for Unit-2</b>			<b>17</b>		

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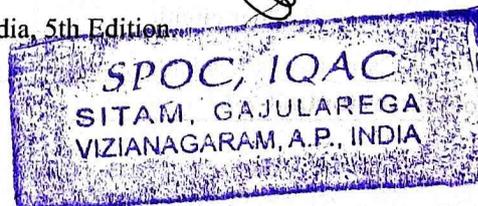
<b>Unit 3: Combinational Logic Circuits Design Using MSI &amp;LSI</b>					
					Chalk and Talk
23	18/04/22	Design of encoder, decoder, multiplexer and demultiplexers	3	T2,R1	Chalk and Talk
24	23/04/22	Implementation of higher order circuits using lower order circuits.	2	T2,R1	Chalk and Talk
25	02/05/22	Realization of Boolean functions using decoders and multiplexers.	3	T2,R1	Chalk and Talk
26	07/05/22	Design of Priority encoder,	1	T2,R1	Chalk and Talk
27	09/05/22	4-bit digital comparator	1	T2,R1	Chalk and Talk
28	10/05/22	Seven segment decoder	1	T2,R1	Chalk and Talk
29	11/05/22	PLDs: PROM, PAL, PLA -Basics structures, realization of Boolean function	3	T2,R1	Chalk and Talk
<b>Total Number of Classes for Unit-3</b>			<b>14</b>		
<b>Unit 4: Sequential Circuits-I</b>					
33	16/05/22	Classification of sequential circuits (synchronous and asynchronous)	2	T1,R3	Chalk and Talk, PPT
34	18/05/22	Operation of NAND & NOR Latches	2	T1,R3	Chalk and Talk, PPT
35	21/05/22	Flip-flops; truth tables and excitation tables of RS flip-flop, JK flipflop, T flip-flop, D flip-flop with reset and clear terminals.	4	T1,R3	Chalk and Talk, PPT
36	25/05/22	Conversion from one flip-flop to another flip-flop	3	T1,R3	Chalk and Talk, PPT
38	30/05/22	Design of synchronous counters	2	T1,R3	Chalk and Talk, PPT
39	01/06/22	Johnson counter, ring counter	1	T1,R3	Chalk and Talk, PPT
40	02/06/22	Design of registers - Buffer register, control buffer register, shift register, bi-directional shift register, universal shift register	3	T1,R3	Chalk and Talk, PPT
<b>Total Number of Classes for Unit-4</b>			<b>17</b>		
<b>Unit 5: Sequential Circuits -II</b>					
46	06/06/22	Finite state machine; state diagrams, state tables, reduction of state tables	2	T2,R4	Chalk and Talk, PPT
47	08/06/22	Analysis of clocked sequential circuits Mealy to Moore conversion and vice-versa.	2	T2,R4	Chalk and Talk, PPT
48	13/06/22	Realization of sequence generator and sequence detector circuits	2	T2,R4	Chalk and Talk, PPT
49	15/06/22	Races and Hazards	2	T2,R4	Chalk and Talk, PPT
<b>Total Number of Classes for Unit-5</b>			<b>8</b>		
<b>Total Number of Classes for all units</b>			<b>69</b>		

**Text Books:**

1. Switching and finite automata theory: ZviKohavi, Niraj K. Jha, Cambridge University Press, 3rd Edition, 2009.
2. Digital Design by Morris Mano, Prentice Hall India, 5th Edition.

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### References:

1. Digital Principles and Applications by Leach , Malvino , Saha, Mc-Graw Hill, 8th Edition, 2014.
2. Switching Theory and Logic Design by A. Anand Kumar, PHI learning, 3rd edition.
3. Introduction to Switching Theory and Logic Design – Fredriac J Hill, Gerald R Peterson, 3rdEdition, John Willey and Sons Inc,
4. Fundamentals of Logic Design by Charles H. RothJr., Cengage Learning, 7th edition,2013

### Course Outcomes:

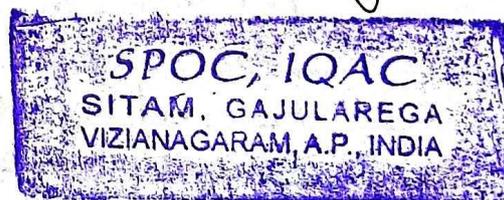
After studying the course, the students are able to

- Classify different number systems and apply to generate various codes.
- Use the concept of Boolean algebra in minimization of switching functions
- Design different types of combinational logic circuits
- Apply knowledge of flip-flops in designing of Registers and counters
- The operation and design methodology for synchronous sequential circuits and algorithmic state machines.

  
Signature of the Faculty

  
Signature of HOD

  
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A glimpse of Course Track Register is enclosed below,

Name of the faculty : Mrs D. vijaya sri  
 Name of the subject : Random variables & stochastic processes  
 Year - Semester - Branch : II - I ECC

date	NO. of hours	Name of the topic	signature
23/2/21	1	UNIT - I: Introduction Review of probability	Sub
25/2/21	1	Definition of Random Variable Conditions of R.V	Sub
26/2/21	2	Types of Random Variable Distribution & Density functions	Sub
27/2/21	1	properties	
30/2/21	1	Binomial, poisson, uniform, Gaussian	Sub
01/3/21	1	Exponential, Rayleigh conditional distribution	Sub
02/3/21	1	conditional density properties	Sub
03/3/21	1	UNIT: II: Introduction	Sub
06/3/21	1	Expected Value of a Random Variable, function of a Random Variable.	Sub
09/3/21	2	Moment about the origin central moments	Sub
10/3/21	2	Variance & skew Chebychev's inequality characteristic function Moment generating function Transformations	Sub

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Date	No. of hours	Name of the topic	Grade
12/11/21	1	Monotonic & non monotonic	2nd
15/11/21	1	Unit III: Vector Random Variables	2nd
16/11/21	2	Joint Distribution function properties, Marginal distribution functions	2nd
18/11/21	1	Conditional distribution and density Statistical Independence	2nd
20/11/21	1	Sum of two Random Variables Sum of several Random Variables	2nd
22/11/21	1	Central limit theorem unequal distribution & equal	2nd
23/11/21	1	joint Moments about the origin joint central moments	2nd
27/11/21	1	joint characteristic functions jointly Gaussian Random Variables	2nd
29/11/21	2	Two Random Variables case, N Random Variables case	2nd
30/11/21	1	Transformation of multiple Random Variables	2nd
7/12/21	2	Linear transformation of Gaussian Random Variables	2nd
11/12/21	1	Unit IV: - The Random process concept classification of processes	2nd
13/12/21	1	Deterministic and Non-deterministic Distribution and density functions	2nd
14/12/21	2	Concept of stationarity and statistical	2nd

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<u>Date</u>	<u>No. of Hours</u>	<u>Name of the topic</u>	<u>Sign.</u>
14/12/21	2	Independence, first-order stationary processes, second & wide-sense " " " $N^{\text{th}}$ -order & strict-sense stationarity	ful
18/12/21	1	Time Averages and Ergodicity.	ful
20/12/21	2	Auto correlation - function and properties cross-correlation - function " "	ful
27/12/21	1	Covariance functions Gaussian Random processes Poisson Random process.	ful
28/12/21	7	<u>UNIT - V</u> :- The power density spectrum properties.	ful
28/12/21	1	Relationship between power density spectrum and Auto correlation function.	ful
29/12/21	1	The cross-power density spectrum properties	ful
03/01/22	1	Relation ship between cross-power density spectrum and cross-correlation function.	ful
21/01/22	2	Random signal Response of linear system convolution, Mean & Mean-squared	ful
25/01/22	2	Auto correlation function of Response cross-correlation functions of i/p & o/p	ful
29/01/22	1	Spectral characteristics of system Response cross-correlation function of i/p and o/p.	ful
31/01/22	1	Power density spectrum of Response,	ful
01/02/22	2	Cross-power spectra of i/p & o/p.	ful

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Sl. No.	Date	No. of slides	Name of the topic	Signature
1	2/02/22	1	Band pass, Band limited & narrow band processes properties.	[Signature]
1	15/02/22	1	<del>Power spectrum</del>	[Signature]
			<del>20/02/22</del>	
			<del>[Signature]</del>	

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 VIZIANAGARAM, A.P., INDIA



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**REMEDIAL CLASSES TIME TABLE (II-II)**

**ACADEMIC YEAR: 2021-22**

	9:20A.M- 10:10A.M	10:10A.M- 11:00A.M	11:00A.M- 11:50A.M	11:50A.M- 12:40P.M	12:40P.M- 01:30P.M	01:30P.M- 02:20P.M	02:20P.M- 03:10P.M	03:10P.M- 04:00P.M	04:00P.M- 04:50P.M
<b>MON</b>					L				M-IV
<b>TUE</b>					U				EDC
<b>WED</b>					N				ECA-II
<b>THU</b>					C				DCMT
<b>FRI</b>					H				EMF
<b>SAT</b>									

SUBJECT CODE	SUBJECT NAME	FACULTY CODE	FACULTY NAME
M-IV	MATHEMATICS-IV	GSC	Mrs.VASANTHA VICHIKALA
EDC	ELECTRONIC DEVICES AND CIRCUITS	VNS	Mrs.V.N.SHIRISHA
ECA-II	ELECTRICAL CIRCUIT ANALYSIS-II	YS	Mr.Y.SANTHOSH KUMAR
DCMT	ELECTRICAL MACHINES-I	PK	Mr.P.KARUNAKAR
EMF	ELECTROMAGNETIC FIELDS	MS	Mrs.M.SWATHI

  
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Few Remedial Class Time tables are attached here under,

<p style="text-align: center;"><b>SITAM</b>  <b>SATYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT</b>                      Gajularega, Vizianagaram, Andhra Pradesh, India-535002.                      Accredited by "NAAC"                      Approved by AICTE and Affiliated to JNTUK, KAKINADA                      Email: sitam@sitam.co.in, Website:www.sitam.co.in                      Telephone No 96767 88811, 897 8812341/2, Land Line: 08922-234775</p>									
<b>REMEDIAL CLASSES TIME TABLE (III-I)</b>									
<b>ACADEMIC YEAR: 2021-22</b>									
09:00A.M- 10:10A.M	10:10A.M- 11:00A.M	11:00A.M- 11:50A.M	11:50A.M- 12:40P.M	12:40P.M- 01:30P.M	01:30P.M- 02:20P.M	02:20P.M- 03:10P.M	03:10P.M- 04:00P.M	04:00P.M- 04:50P.M	
				L				ECA	
				U				LCS	
				N				EMTL	
				C				AC	
				H				CAO	
SUBJECT NAME			FACULTY CODE	FACULTYNAME					
ELECTRONIC CIRCUIT ANALYSIS			TDVA	Dr.T.D.V.ANAIDU					
LINEAR CONTROL SYSTEMS			MS	Mrs.M.SWATHI					
ELECTROMAGNETIC THEORY AND TRANSMISSION LINES			MSR	Mr.M.SRINIVASARAO					
ANALOG COMMUNICATIONS			AVR	Mr.A.VENKATESWARA RAO					
COMPUTER ARCHITECTURE AND ORGANISATION			TAJ	Mr.T.ANJKUMAR					

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